In the Claims

1. (currently amended) A method used to form a semiconductor device comprising:

~~providing~~ forming a semiconductor wafer section comprising first, second, and third pads thereon ~~a bond pad having first and second portions~~ which are electrically separated from each other;

~~providing~~ forming a first circuit portion electrically coupled with said first ~~bond~~ pad ~~portion~~;

~~providing~~ forming a second circuit portion electrically coupled with said second ~~bond~~ pad ~~portion~~ and electrically isolated from said first circuit portion;

forming a third circuit portion electrically coupled with said third pad and electrically isolated from said first and second circuit portions; and

selectively electrically connecting together either said first and second pads ~~portions~~ or said second and third pads to electrically connect either said first and second circuit portions or said second and third circuit portions,

wherein said semiconductor wafer section is enabled to function with a first operational mode if said first and second pads are electrically connected together, and is enabled to function with a second operational mode different from said first operational mode if said second and third pads are electrically connected together.

2. (currently amended) The method of claim 1 further comprising attaching a single ball bond to ~~said first and second bond~~ two of said pads ~~portions~~ during said ~~electrically connecting of said first and second pad portions~~ selective electrical connection.

3. (currently amended) The method of claim 1 further comprising attaching a wire bond to ~~said first and second bond~~ two of said pads ~~portions~~ during said selective electrical connection ~~electrically connecting of said first and second pad portions~~.

4. (currently amended) The method of claim 1 further comprising screen printing a conductive epoxy to ~~said first and second bond~~ two of said pads ~~portions~~ during said selective electrical connection ~~electrically connecting of said first and second pad portions~~.

5. (canceled)

6. (currently amended) The method of claim 1 further comprising:

providing a transistor during said providing of said first circuit portion and providing one of a fuse and antifuse array during said providing of said second circuit portion; and

selectively electrically connecting said first pad with said second pad thereby electrically coupling said one of said fuse and antifuse array to said transistor during said selective electrical connection of said first and second ~~bond~~ pads ~~portions~~.

7. (currently amended) The method of claim 1 further comprising:

providing a lead frame; and

subsequent to selectively electrically connecting either said first and second pads ~~portions~~ or said second and third pads, attaching said wafer section to said lead frame.

8. (original) A method used during the formation of a semiconductor device comprising:

providing first and second conductive pad portions electrically isolated from each other;

providing a transistor electrically coupled with said first conductive pad portion;

providing one of a fuse array and an antifuse array, said array electrically coupled with said second conductive pad portion;

electrically coupling said second pad portion to a voltage source;

with said second pad portion electrically coupled to said voltage source, programming said array; and

subsequent to programming said array, electrically coupling said first pad portion with said second pad portion.

9. (original) The method of claim 8 further comprising electrically coupling said second pad portion to said voltage source through a probe tip during said electrical coupling of said second pad portion with said voltage source.

10. (original) The method of claim 8 further comprising:

providing a CGND node during said providing of said second pad portion;

electrically coupling said CGND node to said transistor during said electrical coupling of said first pad portion with said second pad portion; and

tying said CGND node to ground through said transistor during an operational mode of said semiconductor device subsequent to programming said array.

11. (original) A method used to form a semiconductor device comprising:

providing a semiconductor wafer substrate assembly;

providing a bond pad comprising at least three separate sections electrically isolated from each other, wherein said three sections of said bond pad each overlie said wafer substrate assembly;

providing at least three circuit portions with one circuit portion electrically connected with only one of said bond pad portions;

electrically interconnecting said at least three bond pad sections to electrically connect said at least three circuit portions.

12. (original) The method of claim 11 further comprising:

providing a lead frame; and

subsequent to electrically interconnecting said at least three bond pad sections, attaching said semiconductor wafer substrate assembly to said lead frame.

13. (original) The method of claim 11 further comprising attaching a ball bond to said at least three bond pad sections during said interconnection of said at least three bond pad sections.

14. (original) The method of claim 11 further comprising screen printing a conductive material to contact said at least three bond pad sections during said interconnection of said at least three bond pad sections.

15. (original) A method used to form a semiconductor device comprising:

providing a semiconductor wafer substrate assembly;

providing a plurality of conductive pads electrically isolated from each other;

providing a plurality of circuits wherein each circuit is electrically connected with one of said bond pads;

selecting an operational mode of said semiconductor device by selectively connecting at least two of said plurality of conductive pads to each other to selectively connect at least two of said plurality of circuits.

16. (original) The method of claim 15 further comprising encapsulating said semiconductor wafer substrate assembly subsequent to said selection of said operational mode.

17. (currently amended) A method used during the formation of a semiconductor device comprising:

providing a semiconductor wafer section;

forming first and second spaced conductive pads on said semiconductor wafer section; and

forming first and second internal power buses on said semiconductor wafer section, wherein said first power bus is electrically connected to said first conductive pad and said second power bus is electrically connected to said second conductive pad,

wherein said first and second conductive pads are adapted to be electrically coupled to each other to electrically connect said first power bus with said second power bus.

18. (original) The method of claim 17 further comprising forming a V_{SS} power bus and a V_{SSQ} power bus during said formation of said first and second internal power buses.

19. (original) The method of claim 17 further comprising electrically connecting said first conductive pad with said second conductive pad to electrically connect said V_{SS} power bus with said V_{SSQ} power bus.

20.-23. (canceled)

24. (previously presented) A method used to form a semiconductor device having a hardwired and selectable column address strobe (CAS) latency, comprising:

providing at least one CAS latency select line;

forming at least a first conductive pad electrically coupled with a high potential, a second conductive pad electrically coupled with said CAS latency select line, and a third conductive pad electrically coupled with a low potential; and

selecting a CAS latency by:

forming a conductor to electrically connect said first pad portion with said second pad portion to select a first CAS latency; or

forming a conductor to electrically connect said second pad portion with said third pad portion to select a second CAS latency which is different from said first CAS latency.

25. (previously presented) The method of claim 24 further comprising forming a ball bond during said formation of said conductor which electrically connects only two of said first, second, and third conductive pads together.

26. (previously presented) The method of claim 24 further comprising forming a bond wire during said formation of said conductor which electrically connects only two of said first, second, and third conductive pads together.

27. (previously presented) The method of claim 24 further comprising encapsulating said CAS select line and said first, second, and third conductive pads subsequent to forming said conductor.

28. (new) The method of claim 1 further comprising encapsulating said semiconductor wafer section, wherein said operational mode is fixed subsequent to encapsulating said semiconductor wafer section.

29. (new) A method of manufacturing a semiconductor device comprising:

prior to encapsulation, selectively electrically connecting conductive pads located on a surface of an integrated circuit die to provide an electrically conductive path between the conductive pads, wherein the conductive path determines an operational mode of the semiconductor device; then

encapsulating the semiconductor die in a dielectric material such that the electrically conductive path is not directly accessible from outside the dielectric material.

30. (new) A method of manufacturing a semiconductor device comprising:

determining a desired operational mode for the semiconductor device;

selectively electrically connecting a plurality of conductive pads located on a surface of an integrated circuit die to provide an electrically conductive path between the conductive pads, wherein the conductive path enables the desired operational mode of the semiconductor device; then

encapsulating the semiconductor die in a dielectric material such that the electrically conductive path is not directly accessible by an end user of the semiconductor device.

31. (new) A method for manufacturing a semiconductor device comprising:

forming a semiconductor die comprising:

a first conductive pad electrically connected to a first circuit portion;

a second conductive pad electrically connected to a second circuit portion;

a third conductive pad electrically connected to a third circuit portion,

wherein said first, second, and third circuit portions are incomplete circuits;

selectively electrically connecting either said first and second conductive pads to electrically connect said first and second incomplete circuit portions to provide a first complete circuit and a first device operational mode, or said second and third

conductive pads to electrically connect said second and third incomplete circuit portions to provide a second complete circuit and a second device operational mode,

wherein said semiconductor device is nonfunctional during operation if two of said conductive pads are not electrically connected.

32. (new) The method of claim 31 wherein said first, second, and third conductive pads are adjacently located to each other and said method further comprises placing a single ball bond on either said first and second pads or on said second and third pads during said selective electrical connection.